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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BARRECA, NICOLE M	
ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,760	IRELAND ET AL.	
	Examiner	Art Unit	
	Nicole M Barreca	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32,36-40,42,44-48,50,51,59-61 and 63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *60* is/are allowed.

6)☒ Claim(s) *32, 36-40, 42, 44-48, 50, 51, 59, 61, 63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 32, 36-39, 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford (US6200734) in view of Tanaka (US 5,733,712).

3. Blatchford discloses a method for fabricating semiconductor devices in integrated circuits using photolithography. The semiconductor device comprises substrate 10, field oxides 11 (dielectric) of varying topography, metal layer 18 (reflective), antireflection coating 17 and photoresist layer 16. The layer of metal will ultimately be patterned to gate electrodes when the MOSFET device is formed. The antireflection coating 17 comprises three layers 13-15 of silicon containing oxides such as silicon oxynitrides, each with different indices of refraction (n) and extinction coefficients or absorptions (k). The antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed (col.1, 18-col.2, 64). Antireflective coating 17 comprising 3 layers with different indices of refraction n and extinction coefficients k are used to eliminate the problem of undesirable interference patterns (col.2, 8-32). When there are three antireflection layers, the first antireflection layer 13 is formed with a thickness of 350-450 angstroms (35-45 nm), while the second antireflection layer 15 is formed with a thickness between

150-250 angstroms (15-25 nm). For the first antireflection layer, k1 is between about 1.1-1.9 and for the second antireflection layer, k2 is between about 0.15-0.3. The index of refraction n2 is in the range of 1.7-2.0 (col.4, 49-61). In order to prevent crosslinking between the photoresist layer 16 and the antireflection coating 17, an additional oxynitride layer 19 (dielectric material, cl.37 or insulating layer formed over the second antireflective layer) is formed there between (col.3, 8-15).

Blatchford teaches that in general antireflection layers are used to eliminate the interference patterns caused by the rays reflected by the underlying topography when the photoresist is exposed and specifically that antireflective coating 17 comprises 3 layers with different indices of refraction n and extinction coefficients k in order to eliminate the problem of undesirable interference patterns. The reference however does not explicitly state that the amplitudes of the interfaces are approximately equal and that the phase differences of the reflected radiation from the interfaces mutually cancel when combined or that the phase differences are approximately 180 degrees out of phase. Tanaka teaches that the known antireflection method utilizes light interference to prevent reflection and that it is known that the antireflection method using light interference requires that the reflectivity of the interfaces be equal and of the opposite phase in order to cancel the reflected light from these interfaces (col.1, 37-38, col.2, 1-9). Therefore one of ordinary skill in the art would have to expect that the amplitudes of the interfaces are approximately equal and that the phase differences of the reflected radiation from the interfaces mutually cancel when combined or that the phase differences are approximately 180 degrees out of phase in the method of

Blatchford which uses three antireflective layers with different indices of refraction n and extinction coefficients k in order to eliminate the problem of undesirable interference patterns because Tanaka teaches that it is known that the antireflection method using light interference requires that the reflectivity of the interfaces be equal and of the opposite phase in order to cancel the reflected light from these interfaces.

Blatchford teaches that k1 is between about 1.1-1.9, k2 is between about 0.15-0.3 and n2 is in the range of 1.7-2.0 (col.4, 49-61). Blatchford also teaches that the indices of refraction for the antireflective layers are different, but is silent on the specific index of refraction for the first antireflective layer, n1, (for the embodiment where there are three antireflective layers), and does not disclose that the first index of refraction is approximately 2.1. However Blatchford teaches that the indices of refraction are varied in the three layers by varying the ratio of silane to nitrous oxide during the deposition and are designed to with used with a photoresist layer which is exposed to DUV light in order to avoid destructive interference of the reflected rays, thereby establishing the indices of refraction as result-effective variables. It would have been within the ordinary skill of one in the art to determine the optimal index of refraction for the first antireflection layer in Blatchford by routine experimentation and to have the thickness be approximately 2.1, if required, because Blatchford establishes that the index of refraction is a result-effect variable and the discovery of an optimum value of a result effective variable is ordinary within the skill of the art (*In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

4. Claims 40, 42, 44, 45, 47, 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Tanaka and Fukuda (US 6255151).

5. The teachings of Blatchford and Tanaka have been discussed above. The references teach a structure comprising three antireflection layers having different indices of refraction, a dielectric layer and a photoresist layer for patterning use in the manufacture of a semiconductor device. The references however are silent on the specific semiconductor device being formed and does not disclose that the semiconductor device comprises a memory cell comprising at least two active areas, a gate stack between the active areas, and a capacitor in electrical contact with one of the active areas (cl.40), or that the structure is a DRAM cell comprising first, second and third active areas, first and second gate stacks and first and second capacitors, the first gate stack being formed between the first and second active areas, the second gate stack being formed between the second and third active areas, the first capacitor being in electrical contact with the first active area, the second capacitor being in electrical contact with the third active area, and the second active area being in electrical contact with a bit line (cl.44), or that the capacitors are formed over the gate stacks (cl.45), or that the bit line is formed over the capacitors (cl.47).

Fukuda teaches that memory cells of a DRAM are generally placed at points where a plurality of word and bit lines intersect on a principal surface of the semiconductor substrate in matrix form. Each memory cell comprises one memory cell section (MISFET) and one capacitor electrically connected in series therewith. The memory cell selection is formed within an active region, is surrounded by a device

separation region and comprises a gate oxide, a gate electrode constructed with each word line, and a source/drain pair. Each bit line is placed at an upper portion of the memory cell and is electrically connected to one of the source and drain shared by two adjacent memory cells, while the capacitor is also placed in the upper portion and electrically connected to the other of the source and drain (col.1, 14-33). It would have been obvious to one of ordinary skill in the art to have the structure comprising the semiconductor substrate, three antireflection layers, dielectric layer and photoresist layer in Blatchford in view of Tanaka to additionally include components such as active regions, gate stacks, capacitors and bit lines, arranged as claimed (cl.40, 45, 47), because Fukada teaches that such components in this arrangement are conventional for a memory cell in the art. While Fukuda does not explicitly disclose that there are three active regions that are specifically arranged as claimed in cl.44, the reference does teach that there are a plurality of memory cells and bit and word lines, arranged in series. It would have been within the- ordinary skill of one in the art to determine the exact number of active regions and cells required for the specific device being manufactured because Fukuda teaches that such memory cells and their general structure are known in the art.

With respect to claim 49, Blatchford teaches that k1 is between about 1.1-1.9, k2 is between about 0.15-0.3 and n2 is in the range of 1.7-2.0 (col.4, 49-61). Blatchford also teaches that the indices of refraction for the antireflective layers are different, but is silent on the specific index of refraction for the first antireflective layer (for the embodiment where there are three antireflective layers), and does not disclose that the

first index of refraction is approximately 2.1. However Blatchford teaches that the indices of refraction are varied in the three layers by varying the ratio of silane to nitrous oxide during the deposition and are designed to with used with a photoresist layer which is exposed to DUV light in order to avoid destructive interference of the reflected rays, thereby establishing the indices of refraction as result-effective variables. It would have been within the ordinary skill of one in the art to determine the optimal index of refraction for the first antireflection layer in Blatchford by routine experimentation and to have the thickness be approximately 2.1, if required, because Blatchford establishes that the index of refraction is a result-effect variable and the discovery of an optimum value of a result effective variable is ordinary within the skill of the art (*In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980)).

6. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Tanaka and Fukuda as applied to claim 45 above, and further in view of Chen (US 6140179).

7. While Blatchford in view of Tanaka and Fukuda teach capacitors arranged in the memory cell, the references do not disclose that the capacitors are container capacitors. Chen teaches that crown (or container) capacitors conventional in the art (col.2, 23-27, col.3, 5-6). It would have been obvious to one of ordinary skill in the art to have the capacitor in Blatchford in view of Tanaka and Fukuda be a container capacitor because Chen teaches crown (container) capacitors are conventional in the art.

8. Claim 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Tanaka, Lyons (US 6287959) and Fukuda.

9. The references have been discussed above. Blatchford teaches a structure comprising three antireflection layers of silicon oxynitride having different indices of refraction, a dielectric layer and a photoresist layer for patterning use in the manufacture of a semiconductor device. Blatchford does not disclose that the silicon oxynitride antireflective layers are an etch stop layer. Lyons teaches that silicon oxynitride can be used as both a successful antireflective layer and etch stop (col.2, 34-41, col.4, 42-49). One of ordinary skill in the art would have to expect that the antireflective layers of silicon oxynitride in Blatchford would additionally function as an etch stop layer because Lyons teaches that that silicon oxynitride can be used as both a successful antireflective layer and etch stop.

Blatchford is silent on the specific semiconductor device being formed and does not disclose that the semiconductor device comprises a memory cell comprising at least two active areas, a gate stack between the active areas, and a capacitor in electrical contact with one of the active areas. Fukuda teaches that memory cells of a DRAM are generally placed at points where a plurality of word and bit lines intersect on a principal surface of the semiconductor substrate in matrix form. Each memory cell comprises one memory cell section (MISFET) and one capacitor electrically connected in series therewith. The memory cell selection is formed within an active region, is surrounded by a device separation region and comprises a gate oxide, a gate electrode constructed with each word line, and a source/drain pair. Each bit line is placed at an upper portion of the memory cell and is electrically connected to one of the source and drain shared by two adjacent memory cells, while the capacitor is also placed in the upper portion

and electrically connected to the other of the source and drain (col.1, 14-33). It would have been obvious to one of ordinary skill in the art to have the structure comprising the semiconductor substrate, antireflection layers, dielectric layer and photoresist layer in Blatchford in view of Tanaka and Lyons to additionally include components such as active regions, gate stacks, capacitors and bit lines, arranged as claimed in claim 50 because Fukada teaches that such components in this arrangement are conventional for a memory cell in the art.

10. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Tanaka, Fukada and Podlesny (US 5724299).

11. The teachings of the references have been discussed above. Blatchford teaches a structure comprising three antireflection layers having different indices of refraction, a dielectric layer and a photoresist layer for use in the manufacture of a semiconductor device, while Fukuda teaches the components and arrangement of a conventional memory cell. The references however do not disclose a computer system comprising a processor and a memory comprising at one memory cell comprising the components as claimed. Podlesny teaches that a memory cell array is typically used as memory for a computer system having a processor (col.6, 42-46). It would have been obvious to one of ordinary skill in the art to have the memory cell including the multiple antireflective layers in Blatchford in view of Tanaka and Fukuda as the memory, along with a processor, in order to form a computer system because Podlesny teaches that it is known in the art to use a memory cell array as memory for a computer system having a processor.

12. Claims 61 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blatchford in view of Tanaka and Lyons.

13. The teachings of Blatchford and Tanaka have been discussed above. The references teach a structure comprising three antireflection layers having different indices of refraction, a dielectric layer and a photoresist layer for patterning use in the manufacture of a semiconductor device. The references do not disclose that the silicon oxynitride antireflective layers are an etch stop layer. Lyons teaches that silicon oxynitride can be used as both a successful antireflective layer and etch stop (col.2, 34-41, col.4, 42-49). One of ordinary skill in the art would have to expect that the antireflective layers of silicon oxynitride in Blatchford would additionally function as an etch stop layer because Lyons teaches that that silicon oxynitride can be used as both a successful antireflective layer and etch stop.

Allowable Subject Matter

14. Claim 60 is allowed.

15. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach or suggest an integrated circuit comprising a first silicon dioxide formed over a reflective surface, a first antireflective layer formed over and in contact with the first silicon dioxide, a second antireflective layer formed over and in contact with the first antireflective layer and a second dioxide layer formed over the second antireflective layer.

Response to Arguments

16. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicole M Barreca whose telephone number is 571-272-1379. The examiner can normally be reached on Monday-Thursday (9AM-7PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nicole M Barreca
Examiner
Art Unit 1756

2/18/05